Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20	shinagawa-masatoshi.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:18
L2	96	shinagawa-m.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:18
L3	3297	shinagawa.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:18
L4	20	kawahara-akifumi.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:19
L5	96	kawahara-a.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:19
L6	14794	kawahara.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:19
L7	42	fukushima-tetsuyuki.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:19
L8	493	fukushima-t.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:20
L9	28072	fukushima.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:20

L10	34	kurâta-masakazu.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:20
L11	134	kurata-m.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:20
L12	8638	kurata.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:20
L13	12	komiya-manabu.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:21
L14	51	komiya-m.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:21
L15	6022	komiya.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:22
L16	26431	"matsushita electric industrial".as.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 12:23
L17	8710	((test testing) same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:27

L18	146	((test testing) same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory))) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and ((port input output) same (send sending transmit transmitting receive receiving reception) same (outside external exterior))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:47
L19	146	((test testing bist "built in self test") same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory))) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and ((port input output) same (send sending transmit transmitting receive receiving reception) same (outside external exterior))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:49
L20	473	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:54
L23	3	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information)) and ((bit near3 (length word)) not (largest maximum greatest))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:59
L24	153	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 12:59

L25	11	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information)) and ((pair plural plurality multiple many several numerous multiplicity) with (connection connected connecting) with (line wire land))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 13:02
L26	249	702/118.ccls.	US-PGPUB; USPAT	OR	OFF	2005/12/05 13:03
L27	617	702/117.ccls.	US-PGPUB; USPAT	OR	OFF	2005/12/05 13:07
L28	73	(126 127) and (13 16 19 112 115 116 117 118 119 120 121 122 123 124 125)	US-PGPUB; USPAT	OR	ON	2005/12/05 14:10
L30	0	(126 127) and (drive unit supplies mixed signal port test piece data bit length largest plurality part expectation output nonvolatile memory together).clm.	US-PGPUB	AND	ON	2005/12/05 14:32
L31	0	(126 127) and (interface circuit connect plurality pair connection line corresponding circuit block disconnect CPU microcomputer test mode).clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L32	0	(126 127) and (two nonvolatile memory pluralityoutput test signal piece data testing circuit block control unit allow prohibits outputting).clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L33	0	(126 127) and (acquire plurality piece selection data outside nonvolatile memory microcomputer chip correspondence test store area unique address selecting frequency first clock signal).clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L34	0	(126 127) and (acquire plurality piece designation data outside nonvolatile memory microcomputer chip correspondence test store designation area unique address designating voltage).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L35	0	(126 127) and (current judgment unit judge power supply current applied microcomputer unit exceed designated designation signal output judgment result).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L36	0	(126 127) and (defective signal outside nonvolatile memory microcomputer chip response test result expectation control unit store address predetermined area defective indicating circuit block judged defective testing).clm.	US-PGPUB	AND	ON	2005/12/05 14:34

L37	0	(126 127) and (second test step storing microcomputer unit judged defective first replacing data nonvolatile memory unit testing).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L38	0	(126 127) and (second test step storing data performing testing item plurality nonvolatile memory microcomputer chips decided tested unit).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L39	0	(126 127) and (second test step testing microcomputer unit first nonvolatile memory chip data supplied).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L40	1	(drive unit supplies mixed signal port test piece data bit length largest plurality part expectation output nonvolatile memory together).clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L41	0	(interface circuit connect plurality pair connection line corresponding circuit block disconnect CPU microcomputer test mode). clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L42	0	(two nonvolatile memory pluralityoutput test signal piece data testing circuit block control unit allow prohibits outputting).clm.	US-PGPUB	AND	ON	2005/12/05 14:33
L43	1	(acquire plurality piece selection data outside nonvolatile memory microcomputer chip correspondence test store area unique address selecting frequency first clock signal).clm.	US-PGPUB	AND	ON	2005/12/05 14:34
L44	1	(acquire plurality piece designation data outside nonvolatile memory microcomputer chip correspondence test store designation area unique address designating voltage). clm.	US-PGPUB	AND	ON	2005/12/05 14:35
L45	1	(current judgment unit judge power supply current applied microcomputer unit exceed designated designation signal output judgment result).clm.	US-PGPUB	AND	ON	2005/12/05 14:35
L46	1	(defective signal outside nonvolatile memory microcomputer chip response test result expectation control unit store address predetermined area defective indicating circuit block judged defective testing).clm.	US-PGPUB	AND	ON	2005/12/05 14:35
L47	1	(second test step storing microcomputer unit judged defective first replacing data nonvolatile memory unit testing).clm.	US-PGPUB	AND	ON	2005/12/05 14:35
L48	1	(second test step storing data performing testing item plurality nonvolatile memory microcomputer chips decided tested unit). clm.	US-PGPUB	AND	ON	2005/12/05 14:35
L49	1	(second test step testing microcomputer unit first nonvolatile memory chip data supplied). clm.	US-PGPUB	AND	ON	2005/12/05 14:35

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	70071	g06f019/00.ipc.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/12/05 14:41
L2	8710	((test testing) same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L3	146	((test testing) same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory))) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and ((port input output) same (send sending transmit transmitting receive receiving reception) same (outside external exterior))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L4	146	((test testing bist "built in self test") same (computer micro$computer processor micro$processor dsp (digital adj signal adj processor)) same ((non$volatile near3 (storage register memory)) rom (read adj only adj memory))) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and ((port input output) same (send sending transmit transmitting receive receiving reception) same (outside external exterior))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L5	473	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42

L6	0	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and (((mixed superposed superpositioned superpositioning) with (data signal information)) same ((test$3 near3 (signal data information)) same (bit near3 (length word)) not (largest maximum greatest)))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L7	0	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and ((test$3 near3 (signal data information)) same (bit near3 (length word)) not (largest maximum greatest))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L8	3	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information)) and ((bit near3 (length word)) not (largest maximum greatest))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L9	153	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42

L10	11	((non$volatile near3 (storage register memory)) rom (read adj only adj memory)) and ((storage register memory) near4 (control controller controlling) near4 (unit part section module)) and ((drive driver driving) near3 (unit part section module)) and (output near3 (unit part section module)) and (port input output) and ((mixed superposed superpositioned superpositioning) with (data signal information)) and (test$3 near3 (signal data information)) and ((pair plural plurality multiple many several numerous multiplicity) with (connection connected connecting) with (line wire land))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:42
L11	1	(drive unit supplies mixed signal port test piece data bit length largest plurality part expectation output nonvolatile memory together).clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L12	0	(interface circuit connect plurality pair connection line corresponding circuit block disconnect CPU microcomputer test mode). clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L13	0	(two nonvolatile memory pluralityoutput test signal piece data testing circuit block control unit allow prohibits outputting).clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L14	1	(acquire plurality piece selection data outside nonvolatile memory microcomputer chip correspondence test store area unique address selecting frequency first clock signal).clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L15	1	(acquire plurality piece designation data outside nonvolatile memory microcomputer chip correspondence test store designation area unique address designating voltage). clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L16	1	(current judgment unit judge power supply current applied microcomputer unit exceed designated designation signal output judgment result).clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L17	1	(defective signal outside nonvolatile memory microcomputer chip response test result expectation control unit store address predetermined area defective indicating circuit block judged defective testing).clm.	US-PGPUB	AND	ON	2005/12/05 14:42
L18	186	g06f019/00.ipc. and (L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 L16 L17)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/12/05 14:52